**Course Project Report**

**EE-789D: Power Electronic Converters for EV Charging**

**Designing a PFC circuit in Peak Current Mode Control.**

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**Introduction:** Increasing proliferation of Power Electronics Converters, in the grid system has been associated with degrading power quality in terms of currents and voltages waveforms distortion and power factor degradation. This is mainly due to the non-linear behaviour which contributes to the pollution in power supply at the point of common coupling but as AC electricity is the most convenient forms of energy which can be transmitted, distributed, and generated, power conversion stage is very much necessary to ensure proper power conversion to make it suitable for various industrial and domestic applications. Hence, it is the duty of a Power Electronic Engineer to present a solution to this power supply pollution.

A Power Factor Correction circuit aims at solving these problems of power factor degradation and increased harmonic pollution by utilizing the existing converter circuits such as the boost and buck-boost circuit and create a unity power factor operation to decrease the harmonic pollution at the point of common coupling. Current control is the most common strategy as our focus is to shape the current at input in such a way to achieve UPF operation. The current control techniques that are frequently used employ Average Current Mode Control and Peak Current Mode Control, the aim of this project is to design a PFC circuit and control it using the Peak Current Mode Control.

**Problem Statement:** Design an AC-DC-DC PFC Circuit in Peak Current Mode Control with the following specifications. Input: 230V, 50Hz AC, Output: 400V DC, Power: 3.3kW fs= 25kHz.

and find 1. Voltage and Current Stress of each element and verify it through simulations.

2. Evaluate the dynamic performance by adding a load step.

**Circuit Designing:** A closed loop circuit diagram of the boost converter is given as in figure 1. To begin with we need to design L and C to have CCM mode of operation and suppress output voltage ripples. Then move on to designing the PFC control circuit by implementing a closed loop control over the voltage and current. For this we need to do a small signal modelling of the circuit.

**Design of Boost Inductor:** For a boost converter having CCM operation;

The half peak ripple current across the inductor L is given by

The low-frequency (Average) component of inductor current is given by .

Where, is the emulated resistance.

For, CCM to happen,

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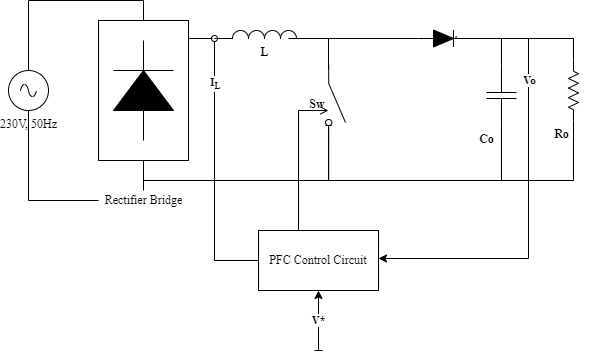


Figure 1 Closed loop PFC Boost Circuit.

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Now, the emulated resistance is given by here, P is the input power which under ideal conditions is equal to output power. For our case P = 3.3kW.

Also,

Here, has a maximum at , and minimum at 0

For CCM to always occur, for our case should be taken as 1. Hence L becomes.

Now, according to our specifications:

Therefore,

Let’s take L for our case to be

**Design of Output Filter Capacitor:**

We know that the instantaneous input power of a single phase-ideal rectifier is not constant and as output is a DC Voltage; input and output powers at any instant must stay same. Therefore, an energy storage element is bound to be added. As inductors tend to be bulky and costly, capacitors are generally used to store the difference between the input and output instantaneous powers. So, if there exists a difference between the two powers the capacitor must be able to discharge the energy over one ac line cycle. Hence, there are designed from the ac line frequency.

So, we can design the capacitor value as.

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Therefor equating the values and let the Peak-to-Peak ripple be limited to 10 volts

Let for our circuit C be equal to 3mF.

**Peak Input Current:**

The peak input current for our circuit will be given by:

Hence for our configuration

**Duty Cycle:**

The duty cycle (D) for our circuit is given by . Hence, D for our configuration will be given by D= 0.18683

**Inner and Outer Loop Transfer Functions:**

We know from the small signal modelling of a boost converter that current to output voltage transfer function is given by: -

And the control to input current transfer function is given by: -

Equating C= 3mF, Vo= 400 V, D=0.18683, R=48.484 Ω, L=0.65 mH, = 20.29A

Hence the transfer functions come out to be:

**Controller Design for Outer Loop:**

The Bode Plot for the current to output voltage transfer function is given by:

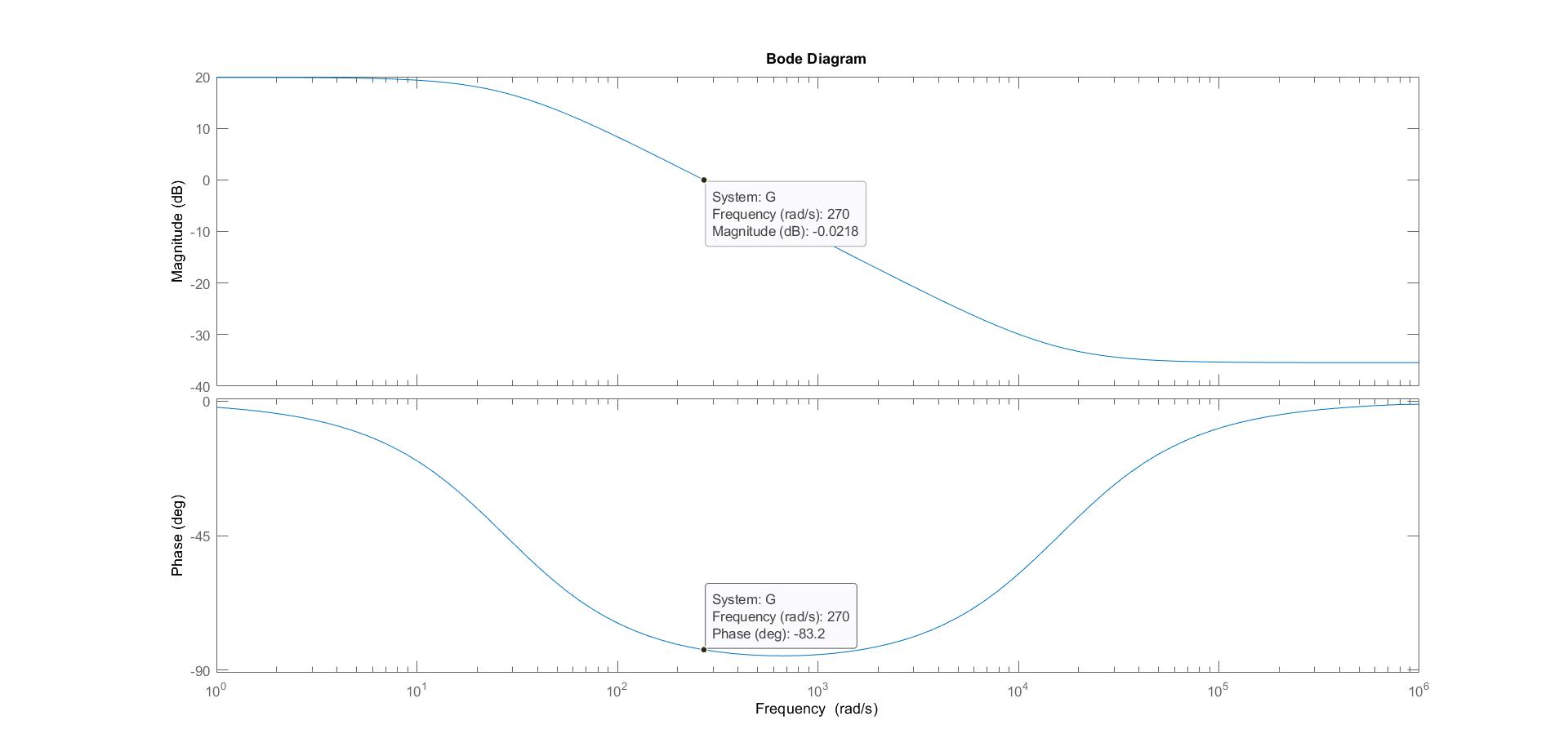


Figure Current-to-Output Voltage Transfer Function

As can be seen our phase margin is stable as it is 180°- 83.2° = 96.8°. But the steady state error is poor as it is only equal to 10%. Hence to improve the steady state error we employ a PI Controller.

Using the help of matlab function pidtune to get the values of and controller transfer function to improve the steady state error of the current-to-output-voltage transfer function.

After tuning and are found to be 0.1268 and 10.6320 respectively and the open loop (GH) bode plot is given as:

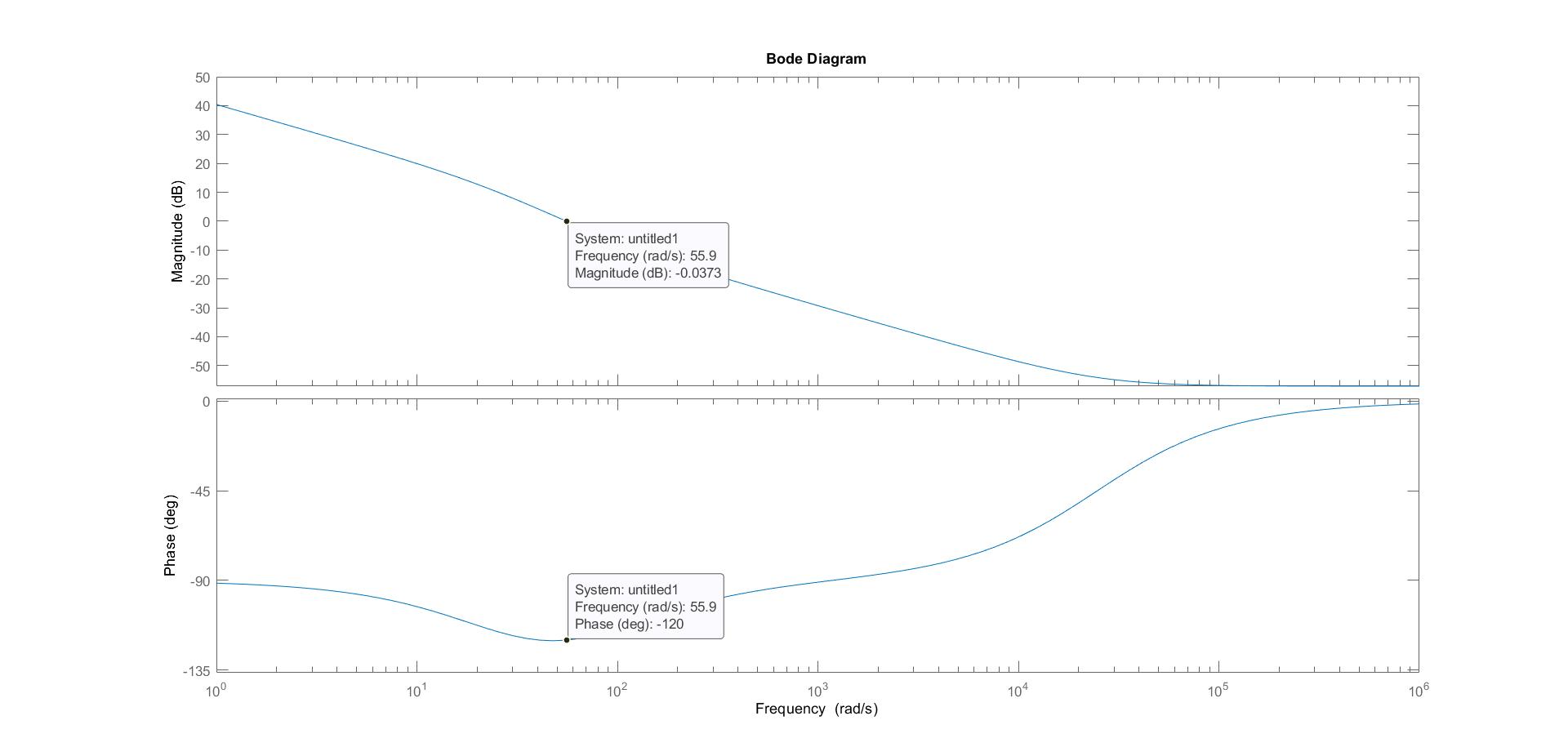


Figure Bode plot of open loop response of outer loop

As can be seen our stead state error has been improved to 1% and the Phase margin is stable at 180°-120° = 60°.

**Controller Design for Inner Loop:**

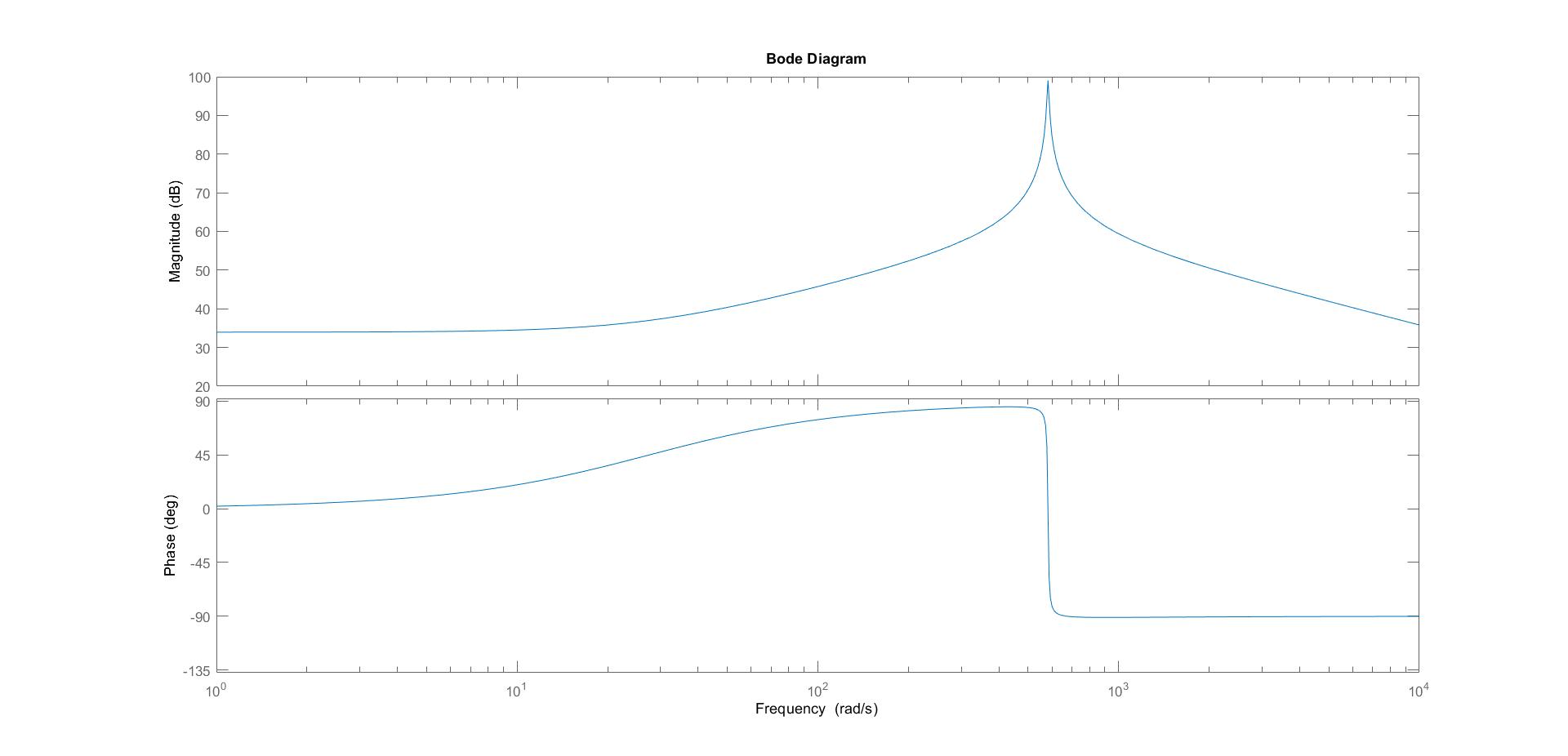
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Figure Bode plot of control-to-input current transfer function

To stabilize the system, we again use the help of matlab function pidtune to get the values of and controller transfer function to improve the steady state error of the current-to-output-voltage transfer function.

and were found to be 8.640 and 212.4 respectively.

**Simulations:**

We run the simulations using the help of MATLAB/SIMULINK;

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Figure Circuit diagram of PFC Boost Topology

The control logic circuitry is made as follows:

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Figure Control Logic Circuitry

Output Voltage waveform as can be seen is stable at 400 V DC output.

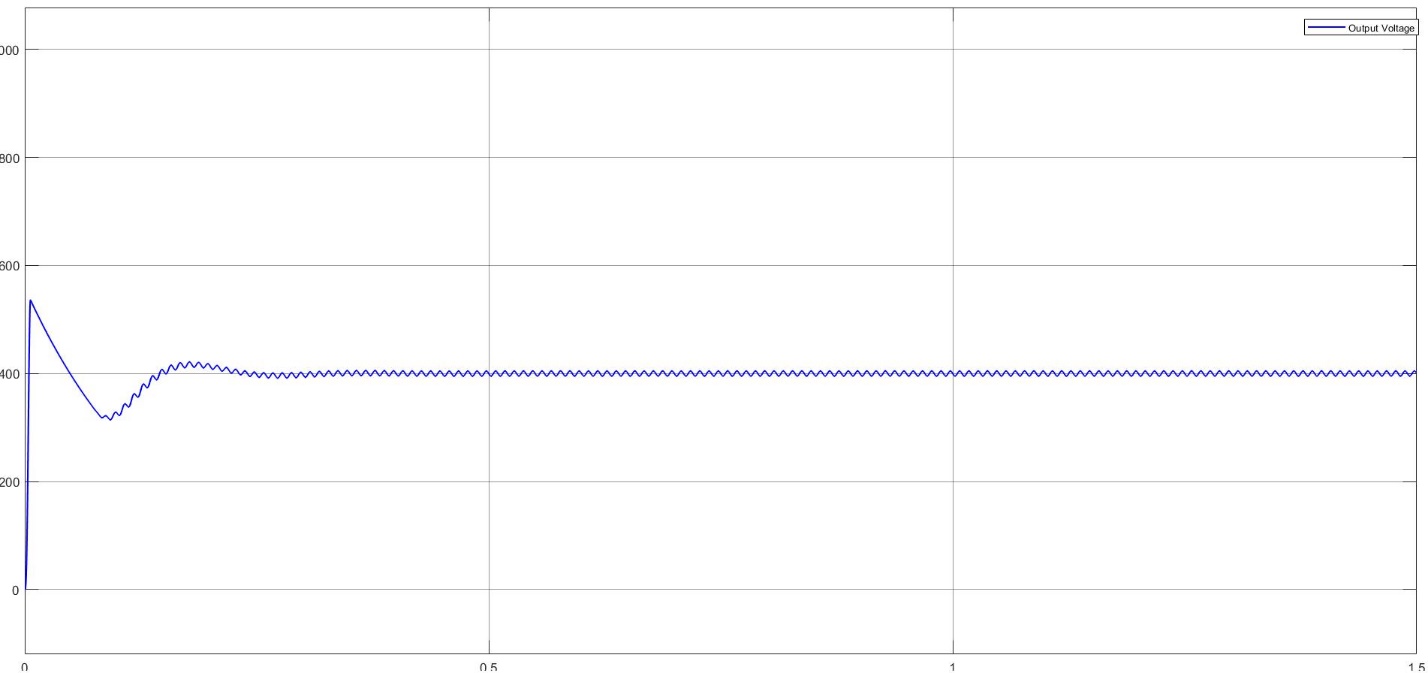


Figure Output Voltage Waveform

Input voltage and current waveform is given by:

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Figure 8 Input Current and Voltage Waveforms

As can be seen the operation at the grid side is at Unity Power Factor and hence our Power Factor Correction circuit is working as it should.

**Current and Voltage Stress of each element:**

Current and Voltage stresses of all the elements are calculated under steady state.

**Current Stress:**

1. **Transistor**: The peak current that passes through the transistor is and the value of which is given by = 20.29 A. This current would also have a ripple associated with it; the ripple is given by 1.87 A. Hence, the peak current stress is given by 22.16 A.

From the Waveform:

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Figure 9 Transistor current waveform

As can be seen the transitor current peak is occurring at around 22.5A, hence, our evaluation is correct.

1. **Inductor:** The peak current that passes through the inductor is and the value of which is given by = 20.29 A. This current would also have a ripple associated with it; the ripple is given by 1.87 A. Hence, the peak current stress is given by 22.16 A.

Diagram

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Figure 10 Inductor Current Waveform

As can be seen the inductor current peak is occurring at around 22.5A, hence, our evaluation is correct.

1. **Diode:**

The peak current that passes through the diode is given by and the value of which comes out to be 20.29 A. This current would also have a ripple associated with it; the ripple is given by 1.87 A. Hence, the peak current stress is given by 22.16 A.

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Figure 11 Diode Current Waveform

As can be seen from the waveform the peak current occurs at 22.5A.

**Voltage Stress:**

1. **Transistor:** The voltage stress around the transistor is the Output Voltage , 400 V(not considering the voltage ripples) when the switch is not in conduction.

**Chart, diagram

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Figure 12 Transistor Voltage Waveform

As can be seen the transistor voltage waveform shows that the Voltage Stress of the Transistor is 400V.

1. **Boost Diode:** The diode when switch is conducting has to block the output voltage. Hence, the Diode Voltage stress is - 400V.

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Figure 13 Diode voltage waveform

The diode voltage stress as can be seen is around – 400V, neglecting output voltage ripples.

1. **Capacitor:**

The capacitor voltage stress is also equal to the output voltage, neglecting voltage ripples.

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Figure 14 Capacitor Voltage

Hence, as can be seen the capacitor voltage stress is 400 V.

**Dynamic Performance:**

We have taken our reference to be 400 V and the output is tracking this reference voltage. Now say that the reference point changes by 50 V. How much time would it take for it to settle at this new reference point is our settling time.

We added a 50 V step to our reference value at 0.45s, then our output voltage settles at this new settling time at:

As can be seen from the figure when the load step was given at 0.45s the output resettles at around 0.518s and hence our settling time comes out to be 68ms.

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Figure Reference point tracking under step.